

3 operation;

4 a second plurality of electronic components defining a non-instant on  
5 mode of operation;

6 a plurality of input/output devices; and

7 one or more switching mechanisms to selectively couple one or more of  
8 said plurality of input/output devices to one or more of said first plurality of  
9 electronic components and enable said apparatus to start up in said instant on  
10 mode of operation to the exclusion of said second plurality of electronic  
11 components, or to selectively couple said one or more input/output devices to  
12 one or more of said second plurality of electronic components and enable said  
13 apparatus to start up in said non-instant on mode of operation to the exclusion of  
14 said first plurality of electronic components.

Sub B3 A2  
1 3. (Amended) The apparatus of claim 2, wherein said first plurality of  
2 electronic components includes a first memory device and said second plurality  
3 of electronic components includes a second memory device, and wherein after  
4 start up said first and second processors operate simultaneously to synchronize  
5 data between said first and second memory devices.

1 4. (Amended) The apparatus of claim 1, wherein at least one of said first and  
2 second plurality of electronic components includes a processor having at least  
3 two operating modes, wherein when in a first operating mode said processor  
4 executes instructions representing a first operating system, and when in a

*a2 cont*  
5. second operating mode said processor executes instructions representing a  
6 second operating system.

*Sub B5*  
8. (Amended) An apparatus comprising:  
an integrated circuit having a plurality of function blocks for use in a first  
instant on mode of operation;  
a plurality of electronic components for use in a second non-instant on  
mode of operation;  
a plurality of input and output devices; and  
one or more switching mechanisms to selectively couple one or more of  
said plurality of input and output devices to one or more of said function blocks to  
enable said one or more input and output devices to be available for use in said  
first instant on mode of operation to the exclusion of said a plurality of electronic  
components, or to selectively couple said one or more of said plurality of input  
and output devices to one or more of said plurality of electronic components to  
enable said one or more input and output devices to be available for use in said  
second non-instant on mode of operation to the exclusion of said plurality of  
function blocks.

*Sub B7*  
*a4*  
11. (Amended) The apparatus of claim 9, wherein said plurality of function  
blocks includes a first memory device, wherein said second plurality of electronic  
components includes a second memory device, and wherein after start up said  
first and second processors operate simultaneously to synchronize data stored

5 within said first and second memory devices.

1 12. (Amended) The apparatus of claim 8, wherein at least one of said plurality  
2 of function blocks and said plurality of electronic components include a processor  
3 having at least two operating modes, wherein when in a first operating mode,  
4 said processor executes instructions representing a first operating system, and  
5 when in a second operating mode, said processor executes instructions  
6 representing a second operating system.

16. (Amended) An integrated circuit comprising:

2 a first processor block to operate in a first instant on mode of operation;

3 a second processor block to operate in a second non-instant on mode of  
4 operation;

5 a plurality of input/output ports; and

6 one or more switching mechanisms to selectively couple one or more  
7 external devices to said first processor block through at least one of said plurality  
8 of input/output ports to facilitate use of said one or more external devices in said  
9 instant on mode of operation to the exclusion of said second processor block, or  
10 to selectively couple said one or more external devices to said second processor  
11 block through at least one of said plurality of input/output ports to facilitate use of  
12 said one or more external devices in said non instant on mode of operation to the  
13 exclusion of said first processor block.

Sub B10  
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18. (Amended) The integrated circuit of claim 16, wherein said plurality of  
2 external devices includes a first memory device and a second memory device,  
3 and wherein after start up said first and second processor blocks operate  
4 simultaneously to synchronize data between said first and second memory  
5 devices.

1 21. Cancelled without prejudice.